REMARKS

This Amendment is submitted in response to the Office Action dated July 7, 2004, having a shortened statutory period set to expire October 7, 2004. In the present Amendment, Claims 19-22 are entered. Claims 1-22 are now pending.

Claim Objections

On page 2, paragraph 3 of the present Office Action, Examiner objected to Claims 1-18 because of certain informalities. Applicant has amended the claims to address these objections and for stylistic reasons.

Claim Rejection Under 35 U.S.C. § 102

In the present Office Action, Claims 1-8 and 10-17 are rejected under 35 U.S.C. § 102(b) as being anticipated by *Chen* (U.S. Patent No. 5,850,422). After careful consideration of Examiner's remarks, Applicant respectfully submits that Claims 1-8 and 10-17, as now amended, are not rendered unpatentable by *Chen* and respectfully traverses Examiner's rejection in view of the arguments submitted herein.

Chen teaches the generation of a recovered clock signal based on a selected clock phase. *Chen's* method for recovering the clock signal includes the following steps: (1) an incoming data stream is provided to the data sampler (Abstract); (2) the data sampler selects one out of several clock phases that is closest to the incoming data stream (col. 2, lines 32-35); (3) a recovered clock signal is generated from the selected clock phase (col. 2, lines 30-35); (4) the data sampler circuit is disabled after the recovered clock signal is generated to save power (col. 8, lines 10-12); (6) the recovered clock signal is monitored to determine if it continues to be an acceptable representation of the clock embedded in the data stream (Abstract); and (7) if not, the process is repeated starting at step 2 (col. 7, lines 11-5 and lines 48-55).

Turning now to the claims, *Chen* does not render exemplary Claim 1 unpatentable because *Chen* does not teach or suggest:

generating a plurality of retimed states by logically combining said plurality of multiphase clock signals and said data stream, wherein said data stream operates at a second clock rate, wherein said second clock rate is an integer N times faster than said first clock rate, wherein said integer N is at least 2.

This feature of the present invention allows a clock signal to be recovered from the data stream from multiphase clock signals operating at a factor of N times slower than the data stream (specification, page 15, lines 14-27, **Figure 13**). This clock recovery scheme enables the operation of the phase-lock loop at lower speeds, which results in power savings, higher densities, and the utilization of less-advanced technologies (specification, page 15, lines 14-27).

In contrast, the apparatus and method disclosed in *Chen* differs significantly from the present invention. For example, with reference to **Figure 3** and col. 4, lines 16 in *Chen*, the voltage control oscillator (VCO) generates multiphase clock signals as the same frequency as the data rate, but out of phase with the incoming data 46. Also, as referenced earlier, the power conservation feature disclosed in *Chen* is implemented by disabling data sampler 14 after the initial phase acquisition, not by operating the multiphase clock signals at a lower speed, as in the present invention.
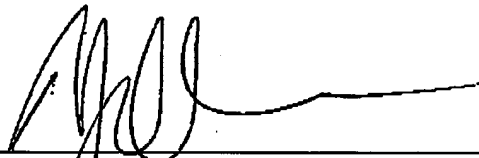
In light of the preceding arguments, Applicant believes that independent Claim 1 similar Claim 10 and all dependent claims are not anticipated by *Chen*.

Applicant has entered four claims (Claims 19-22) that clarify how specific multiphase clock signals are selected and how the retimed data signal is generated in response to the retime states. Support for this feature can be found in the **Figure 13** and the corresponding discussion in the Specification on page 15, lines 7-27 of the pending application. Note that the retime states are logically combined (AND block) with multiphase clock signals to select a phase to correspond to the retimed data (**Figure 13**). Upon review of *Chen*, nothing in *Chen* teaches or suggests the selection of multiphase clock signals to correspond to a retimed data signal generated in response to retime states.

Please charge $36.00 to **IBM Corporation Deposit Account Number 09-0447** for the additionally added claims. No additional fee is believed to be required. However, in the event that any additional fee is required, please charge that fee to **IBM Corporation Deposit Account Number 09-0447.**

Applicant respectfully requests the Examiner contact the undersigned attorney of record at (512) 343-6116 if such would further or expedite the prosecution of the present Application.

Respectfully submitted,

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